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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,430	03/09/2004	Chin-Shan Hou	252016-2660	1867

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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,430	HOU ET AL.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,11-15,19,21 and 22* is/are rejected.

7)☒ Claim(s) *6-8,10,16-18,20 and 23-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *29/04/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is with regards to Application No. 10/796,430 filed 09 March 2004. Claims 1 0 25 are pending in this Application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims1 – 4 and 11 – 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Mau (U.S. Patent No. 6,532,570 B1).

4. Referring to claim 1, Mau discloses a method to optimize a signal routing (interconnections) in an IC (see col. 2, line 65 – col. 3, line 7; col. 3, line 65 – col. 4, line 23) comprising:

(a) providing a signal routing in an IC layout wherein the signal routing (interconnections) comprises a configuration of metal lines in a stack of metal levels and wherein each metal level is separated from an underlying substrate by dielectric material (see col. 1, ll. 22 – 25; col. 3, line 65 – col. 4, line 11);

(b) thereafter calculating a Joule heating estimate (it is well known that Joule heating is proportional to current density) for the signal routing (see col. 4, ll. 12 – 22);

(c) thereafter comparing the Joule heating estimate to a standard value (i.e., meet a reliability criteria or goal) – see col. 4, ll. 12 – 36 and Figs. 7A – D;

(d) thereafter updating signal routing if the Joule heating estimate exceeds standard value wherein the updating comprises generating a new configuration of metal lines in the metal levels, and wherein the new configuration reduces the Joule heating (see again Figs. 7A – D; col. 8, line 48 - col. 10, line 15); and

(e) thereafter repeating the steps of calculating, comparing and updating if the Joule heating estimate still exceeds the standard value (see Figs. 7A – D; col. 8, line 48 – col. 10, line 15).

Thus, Mau clearly teaches all the claimed limitations.

5. As to claim 2, see col. 2, ll. 1 – 10, which cites how copper can also be used in the IC interconnections.

6. Pursuant to claim 3, see col. 3, line 65 – 23, which teach the element of the "layout phase of the design". It is well known in the art of complex IC design that signal routing in a circuit layout is always performed by an automated routing system.

7. As per claim 4, see col. 8, ll. 15 – 23, which shows how the Joule heating is based on current density in a metal line and thermal conductivity (i.e., thermal resistance) of between the metal line and the substrate (i.e., dielectric material), as claimed.

8. Regarding claim 11, Mau teaches a method to design an IC device (see Abstract; col. 1, ll. 17 – 20) comprising:

(a) generating an IC layout wherein the signal routing (interconnections) comprises a configuration of metal lines in a stack of metal levels and wherein each metal level is separated from an underlying substrate by dielectric material (see col. 1, ll. 22 – 25; col. 3, line 65 – col. 4, line 11);

(b) thereafter calculating a Joule heating estimate (it is well known that Joule heating is proportional to current density) for the signal routing (see col. 4, ll. 12 – 22);

(c) thereafter comparing the Joule heating estimate to a standard value (i.e., meet a reliability criteria or goal) – see col. 4, ll. 12 – 36 and Figs. 7A – D;

(d) thereafter updating signal routing if the Joule heating estimate exceeds standard value wherein the updating comprises generating a new configuration of metal lines in the metal levels, and wherein the new configuration reduces the Joule heating (see again Figs. 7A – D; col. 8, line 48 - col. 10, line 15); and

(e) thereafter repeating the steps of calculating, comparing and updating if the Joule heating estimate still exceeds the standard value (see Figs. 7A – D; col. 8, line 48 – col. 10, line 15).

Thus, Mau clearly discloses all the limitations as claimed.

9. Claims 12 – 14 contain the same limitations found in claims 2 – 4, respectively, and thus the same rejections also apply.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 5 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Mau in view of Yokogawa (U.S. Patent No. 6,816,995 B2).

Mau teaches a method to design an IC device, and a method to optimize a signal routing in an IC, by calculating Joule heating estimates for the interconnections and updating/repairing signal routing that do not meet certain criteria. Mau also teaches the use of copper for routing.

However, Mau is silent on forming the metal lines using a damascene process.

Yokogawa teaches a method of designing interconnects that include copper interconnects that use the damascene process to form the copper interconnects.

Since, as stated by Yokogawa (col. 1, ll. 22 – 33), the damascene technology is widely used when copper is the interconnect metal because it is difficult to etch thin films of copper that have been formed, it would therefore be obvious to a person of ordinary skill in the art at the time of the invention to combine the teachings of Mau and Yokogawa to obtain the same claimed invention.

12. Claims 9, 19, 21 and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Mau in view of U.S. Patent No. 6,604,228 B1 to Patel et al.

Referring to claim 21, Mau teaches a method to design an IC device, and a method to optimize a signal routing in an IC, by calculating Joule heating estimates for the interconnections and updating/repairing signal routing that do not meet certain criteria.

But Mau does not disclose include using a heat sink coupled to a first set of metal lines.

Patel et al. however disclose a technique of fabricating an IC that may be used in different operating modes depending on a selected option (see Abstract) that includes a heat sink coupled to a first metallization layer in order to dissipate heat to improve circuit reliability (see Figs. 14 and 15; col. 22, ll. 17 – 27).

Since, as stated by Patel et al. (col. 22, ll. 17 – 28), using a heat sink draws heat away from hot spots in the IC and thus improve circuit reliabilty, it would therefore be obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Mau and Patel et al., to achieve the same claimed invention.

13. As per claims 9, 19 and 22, see Fig. 15; col. 22, ll. 25 – 28, which teach the claimed limitation of using metal fingers (i.e., a large thermal mass) to create the heat sink.

Allowable Subject Matter

14. Claims 6 – 8, 10, 16 – 18, 20 and 23 – 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter: these claims contain certain limitations pertaining to dielectric material volume, as well as diffusion regions and doping of the substrate that are not disclosed in the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
18 April 2006

A. M. Thompson
Primary Examiner
Technology Center 2800